AMENDMENTS TO THE CLAIMS

Please amend claim 29. No new matter is believed to be introduced by the aforementioned amendment. The following listing of claims will replace all prior versions and listings of claims in the application:

1. **(Original)** An integrated circuit for use in a transceiver module, the integrated circuit comprising:

a first electrical input port for receiving a first serial electrical data stream;

receiver eye opener circuitry for retiming and reshaping the first serial electrical data stream;

a first electrical output port for transmitting the retimed and reshaped first serial electrical data stream to external to the integrated circuit;

a second electrical input port for receiving a second serial electrical data stream from external to the integrated circuit;

transmitter eye opener circuitry for retiming and reshaping the second serial electrical data stream; and

a second electrical output port for transmitting the retimed and reshaped second serial electrical data stream.

2. **(Original)** The integrated circuit of claim 1 further comprising:

eye opener control circuitry coupled to at least one of the eye opener circuitries for controlling operation of the eye opener circuitry.

3. **(Original)** The integrated circuit of claim 2 wherein the eye opener control circuitry includes clock polling control circuitry for polling a clock frequency on at least one of the eye opener circuitries.

4. **(Original)** The integrated circuit of claim 2 wherein the eye opener control circuitry includes polarity control circuitry for selectably controlling a polarity of at least one of the serial electrical data streams received or transmitted by the eye opener circuitries.

5. **(Original)** The integrated circuit of claim 2 wherein the eye opener control circuitry includes baudrate control circuitry for adjusting a baudrate response of at least one of the eye opener circuitries.

6. **(Original)** The integrated circuit of claim 2 wherein the eye opener control circuitry includes power management circuitry for managing power consumed by the eye opener circuitries and related components on the integrated circuit.

7. **(Original)** The integrated circuit of claim 2 wherein the eye opener control circuitry includes a serial interface for communication between the eye opener control circuitry and external to the integrated circuit.

8. **(Original)** The integrated circuit of claim 2 wherein the eye opener control circuitry includes a serial bus interface for communication between the eye opener control circuitry and external to the integrated circuit according to a predetermined bus protocol.

9. **(Original)** The integrated circuit of claim 1 further comprising:

eye opener communication circuitry for facilitating communication between the receiver eye opener circuitry and the transmitter eye opener circuitry.

10. **(Original)** The integrated circuit of claim 9 wherein the eye opener communication circuitry detects for failure of eye opener circuitry.

11. **(Original)** The integrated circuit of claim 1 further comprising a reference clock port for receiving a reference clock from external to the integrated circuit, the reference clock for clocking both the receiver eye opener circuitry and the transmitter eye opener circuitry.

12. **(Original)** The integrated circuit of claim 1 wherein the transmitter eye opener circuitry is coupled to receive a clock recovered by the receiver eye opener circuitry from the second serial electrical data stream, the received clock for clocking the transmitter eye opener circuitry.

13. **(Original)** The integrated circuit of claim 1 further comprising:

a post-amplifier for a receiver, the post-amplifier coupled to transmit an amplified first serial electrical data stream to the receiver eye opener circuitry.

14. **(Original)** The integrated circuit of claim 13 further comprising:

a digital-to-analog converter (DAC) for converting a digital control signal to an analog control signal, the analog control signal for use in controlling the post-amplifier.

15. **(Original)** The integrated circuit of claim 1 further comprising:

a driver for a transmitter, the driver coupled to receive the second serial electrical data stream from the transmitter eye opener circuitry.

16. **(Original)** The integrated circuit of claim 15 further comprising:

a digital-to-analog converter (DAC) for converting a digital control signal to an analog control signal, the analog control signal for use in controlling the driver.

17. **(Original)** The integrated circuit of claim 1 wherein each serial electrical data stream has a data rate of approximately 10 Gb/s or faster.

18. **(Original)** The integrated circuit of claim 1 wherein the retimed and reshaped first serial electrical data stream comprises an XFI (10 Gb/s serial electrical interface)-compliant electrical data stream, and the second serial electrical data stream comprises an XFI-compliant electrical data stream.

19. **(Original)** The integrated circuit of claim 1 further comprising:

a digital-to-analog converter (DAC) for converting a digital control signal to an analog control signal, the analog control signal for use in controlling the integrated circuit.

20. **(Original)** The integrated circuit of claim 19 wherein the analog control signal is for use in controlling operation of at least one of the eye opener circuitries.

21. **(Original)** In an integrated circuit for use in a transceiver module, a method of communicating data comprising, within the integrated circuit:

receiving a first serial electrical data stream;

retiming and reshaping the first serial electrical data stream;

transmitting the retimed and reshaped first serial electrical data stream to external to the integrated circuit;

receiving a second serial electrical data stream from external to the integrated circuit;

retiming and reshaping the second serial electrical data stream; and

transmitting the retimed and reshaped second serial electrical data stream.

22. **(Original)** An integrated circuit for use in a transceiver module, the integrated circuit comprising:

first eye opener means for retiming and reshaping a received first serial electrical data stream;

output means for transmitting the retimed and reshaped first serial electrical data stream to external to the integrated circuit;

input means for receiving a second serial electrical data stream from external to the integrated circuit; and

second eye opener means for retiming and reshaping the second serial electrical data stream.

23. **(Original)** The integrated circuit of claim 22 further comprising:

control means coupled to at least one of the eye opener means for controlling operation of the eye opener means.

24. **(Original)** The integrated circuit of claim 22 further comprising:

communication means for facilitating communication between the first eye opener means and the second eye opener means.

25. **(Original)** An integrated circuit for use in a transceiver module, the integrated circuit comprising:

a plurality of power-consuming circuitries, comprising

receiver eye opener circuitry for retiming and reshaping a first serial electrical data stream;

transmitter eye opener circuitry for retiming and reshaping a second serial electrical data stream; and

optionally, at least one eye opener related circuitry that is related in operation to the eye opener circuitries;

power management circuitry for selecting a power mode for at least a portion of one of the power-consuming circuitries;

a first electrical output port for transmitting the retimed and reshaped first serial electrical data stream to external to the integrated circuit; and

a second electrical input port for receiving the second serial electrical data stream from external to the integrated circuit.

26. **(Original)** The integrated circuit of claim 25 wherein the power management circuitry selects the power mode according to a start-up protocol.

27. **(Original)** The integrated circuit of claim 25 wherein the power management circuitry selects the power mode in response to a command received from external to the integrated circuit.

28. **(Original)** The integrated circuit of claim 25 wherein the power management circuitry automatically switches the power mode for at least one power-consuming circuitry during normal operation of the integrated circuit.

29. **(Currently Amended)** The integrated circuit of claim 25 wherein the power management circuitry powers down the transmitter eye opener circuitry when the integrated circuit operates as a transmitter rather than as a transceiver.

30. **(Original)** The integrated circuit of claim 25 wherein the retimed and reshaped first serial electrical data stream comprises an XFI (10 Gb/s serial electrical interface)-compliant electrical data.